NAME

Clara Schaertl Short - eclectical engineer returning from sabbatical

SYNOPSIS

cu -c "+1 (310) 237-2826"
mail -s "Your resume" clara@cshort.io
curl https://cshort.io/clarity.7 | **mandoc**

DESCRIPTION

Clara Short (they/them or she/her) is a hardware engineer who *happens* to mostly write software these days: most recently, tools for bringing up, validating, and using the new Design for Debug (DFD) features on the next generation of phone and laptop SoCs. In other words, they use their training as an EE to make hardware debugging easier for software engineers. Their favorite method of building trust with other teams is to start submitting pull requests for features their own team needs.

This year Clara took a short break to work on personal projects, and semi-accidentally ended up turning one of them into a commercial product (pending launch).

EXAMPLES

September 2025 - present: Owner, Autonoë Systems LLC, Medford, MA

- Designed a low-cost AMD UltraScale+ FPGA development board with 28 Gbps expansion ports.
- Created demo workloads exercising PCI Express, 100 Gigabit Ethernet and DDR4 SDRAM.
- Debugged signal integrity/power integrity issues on early revisions with minimal lab tools.
- Released all design files as open-source hardware.
- Launching on Crowd Supply in winter 2025-26.

July 2019 - April 2025: Silicon Validation Engineer, Apple Inc., Waltham, MA

- Responsible for silicon bringup and validation of Apple's cross-triggering network on each SoC.
- Created tools to extract DFD architecture information directly from the RTL design.
- Extended the OS kernel, boot loader, and SoC debugger to enable new validation use cases.
- Trained triage engineers in tool usage and provided hands-on support during bringup and debug.
- Led discussions with IP designers and software teams about future requirements.

May 2018 - August 2018: Silicon Validation Intern, Apple Inc., Austin, TX

- Wrote the collateral extraction tool for a new DFD feature, saving 20 engineer-hours per stepping.
- Re-implemented SoC debugger support for the new feature to streamline collateral delivery.

June 2014 - December 2017: Control Systems Engineer, Mangan Inc., Long Beach, CA

- Designed and commissioned Programmable Logic Controller (PLC) systems in oil refineries.
- Created the client's standard software library for process analyzer PLCs.

- Introduced a tool for semi-automatic PLC software validation, saving 80 engineer-hours per project.
- Independently managed projects up to $5,000.

May 2009 - May 2014: Submarine Officer, United States Navy, Kings Bay, GA

- Shift supervisor for operations, maintenance, and testing of a nuclear submarine with a crew of 160.
- Line manager for 12 electricians and electronics technicians.

COMPATIBILITY

Clara works best in a collaborative environment, where there’s a culture of engineers regularly looking at each other’s work and occasionally pairing on tricky problems. They prefer distributed, cross-functional organizations where accountability is everywhere but "ownership" is a dirty word - see above re: their habit of trading pull requests with other teams.

Clara works in the Greater Boston area and can travel up to one week per quarter for hardware bringups.

STANDARDS

- Fluent in Python and C.
- Conversational in C++, Tcl(n), sh(1), and SystemVerilog.
- Proficient with AMD FPGA toolchains, JTAG, and IEEE 1500.

HISTORY

August 2017 - May 2019: M.S. Electrical and Computer Engineering

University of Texas at Austin, Austin, TX.

June 2005 - May 2009: B.S. Electrical Engineering

United States Naval Academy, Annapolis, MD.